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# Monolithic integration of resonant interband tunneling diodes and high electron mobility transistors in the InAs/GaSb/AlSb material system

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InAs/AlSb high electron mobility transistors (HEMTs) and resonant interband tunneling diodes (RITDs) with AlSb barriers and GaSb wells were grown in a single heterostructure by molecular beam epitaxy. The resulting HEMTs exhibit excellent dc and microwave performance at low drain voltages, with an intrinsic unity-current-gain cutoff frequency of 220 GHz. The RITD performance is comparable to RITDs grown directly on InAs substrates, with peak current densities above  $10^4$  A/cm<sup>2</sup> and peak-to-valley ratios near 11 for 15 Å AlSb barriers. The results represent an important step toward the fabrication of high-speed, low-power logic circuits in this material system. [S0734-211X(00)02003-5]

## I. INTRODUCTION

Digital circuits operating at speed approaching 100 GHz with low power consumption are required for applications in multifunction radar and communication systems. An attractive approach to achieve the required speed with reduced power dissipation is to integrate resonant interband tunneling diodes (RITDs) or resonant tunneling diodes (RTDs) and high electron mobility transistors (HEMTs). This combination enables designs with very high functionality due to the self-latching nature of RTD or RITD circuits. RTD/HEMT circuits have been fabricated in the InP-based material system for low-power static random access memory<sup>1</sup> and logic gates operating at 35 GHz.<sup>2</sup>

The 6.1 Å material system, consisting of InAs, GaSb, AlSb, and related alloys, offers the potential for RITD/HEMT circuits operating at lower power than the InP-based circuits. Specifically, HEMTs with InAs channels and AlSb barriers operating at a drain voltage of only 100 mV exhibit measured unity-current-gain cutoff frequencies of 90 GHz, the highest value reported for any field-effect transistor at this low voltage.<sup>3</sup> The substantial flexibility for band gap engineering in the 6.1 Å system offers the ability to make RITDs with high peak currents at low bias voltages. For example, Chow *et al.* reported peak currents of  $3 \times 10^4$  A/cm<sup>2</sup> at biases near 100 mV.<sup>4</sup> As a result, digital logic circuits based upon integration of the 6.1 Å HEMT and RITD should be able to operate at lower clock voltages than InP-based RTD/HEMT circuits.<sup>2</sup> We note that InAs/AlSb/GaSb Schottky barrier/RITD logic circuits have been demonstrated to 12 GHz, the frequency limit of the test equipment.<sup>5</sup> In addition, Shen *et al.* reported the successful integration of GaAs-based field-effect transistors and 6.1 Å RITDs in a logic gate.<sup>6</sup>

A first step toward the integration of Sb-based HEMTs and RITDs into digital circuits is the epitaxial growth of heterostructures containing both devices. In this article, we discuss the growth of RITD/HEMT structures by molecular beam epitaxy (MBE) and demonstrate that high-performance

HEMTs and RITDs can be fabricated in a single heterostructure.

## II. EXPERIMENT

A cross section of our complete heterostructure is shown in Fig. 1. In simplest terms, it consists of an RITD grown on top of a HEMT. Starting from the semi-insulating GaAs substrate: The AlSb buffer layer accommodates the 7%–8% lattice mismatch between the InAs/AlSb/GaSb materials and the GaAs. The  $p^+$  GaSb layer is intended to drain a portion of the impact-ionization-generated holes back to the source contact rather than allowing them to remain in the AlSb buffer layer and cause deleterious trapping effects. The larger band gap subchannel serves to reduce impact ionization by allowing electrons to transfer from the InAs channel to the subchannel before gaining enough kinetic energy for impact ionization.<sup>7</sup> Modulation doping is achieved by charge transfer from an extremely thin (4 monolayer) Si-doped InAs layer located above the channel.<sup>8</sup> A lattice-mismatched (~4%) In<sub>0.4</sub>Al<sub>0.6</sub>As layer provides a barrier for hole transport between the channel and gate.<sup>3,9</sup> This layer also enables the use of a gate recess etch into the upper barrier material prior to gate metal definition. The energy band diagram for the HEMT was obtained from a self-consistent calculation for  $V_{GS}=0$  and is shown in Fig. 2.<sup>7</sup> The 1000–2000 Å  $n^+$ InAs layer above the antimonide-based etch stop reestablishes a lattice constant of 6.1 Å prior to the RITD growth. The reflection high-energy electron-diffraction pattern degrades during the InAlAs layer, with spots indicative of a three-dimensional growth mode, and recovers during the InAs layer. The doped and undoped InAs layers serve as contacts for the RITD, which contains AlSb tunneling barriers and a GaSb well. The type-II band alignment is shown in Fig. 3. Interband tunneling through the structure occurs when electrons from the InAs conduction band tunnel through the AlSb barrier, into the GaSb valence band, through the second barrier, and into the InAs conduction band. This is in contrast to resonant tunneling in a heterostructure with a type-I band alignment where the electrons tunnel via conduction band states in the well.

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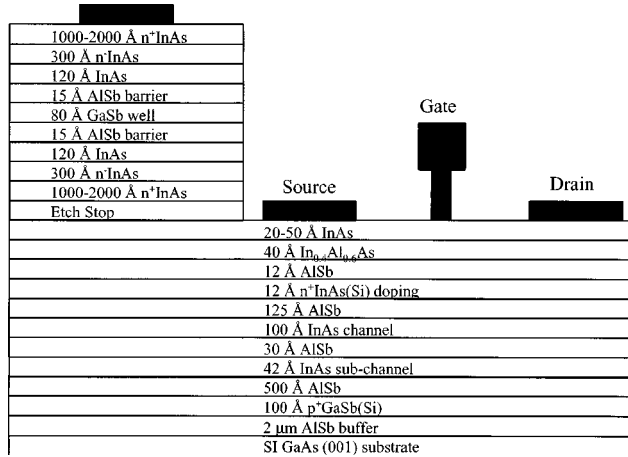


FIG. 1. Cross section of RITD/HEMT structure.

Samples were grown by solid-source MBE using  $\text{As}_2$  and  $\text{Sb}_4$ , with growth rates that varied from 0.4 to 1.0 ML/s. Substrate temperatures were measured by transmission thermometry<sup>10</sup> and ranged from 400 to 550 °C (see Sec. III). V:III flux ratios were between 1.5:1 and 2:1. The As valve was closed during all AlSb and GaSb layers to minimize As incorporation. Migration-enhanced epitaxy was used at interfaces between InAs and AlSb to achieve InSb-like bonds.<sup>11</sup>

Standard photolithography procedures were used to fabricate an array of Ti/Pt/Au ohmic contacts that also serve as an etch mask for the formation of mesa RITDs with diameters of 1.2–50  $\mu\text{m}$ . Prior to the start of the HEMT fabrication process, the RITD material was removed by selective wet etchants. The HEMT source and drain contact patterns were defined using a poly(methylmethacrylate) (PMMA) resist and deep-ultraviolet lithography. Pd/Pt/Au layers ( $\sim 120$  Å/210 Å/600 Å) were deposited by e-beam evaporation and heat treated for 3 h at 175 °C. After ohmic contact formation, a Cr/Au Schottky gate was formed using PMMA e-beam lithography and lift-off techniques. The recess etch through the cap layer was performed with a citric acid-based etch prior to gate metal deposition. Finally, device isolation was

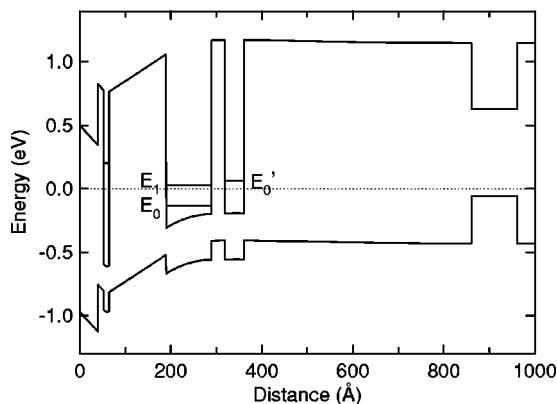
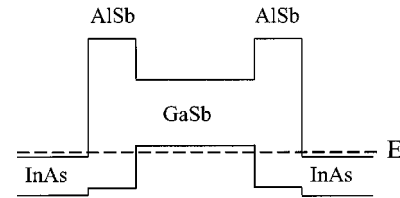


FIG. 2. Calculated band structure for InAs/AlSb HEMT at zero bias and 300 K (from Ref. 7).

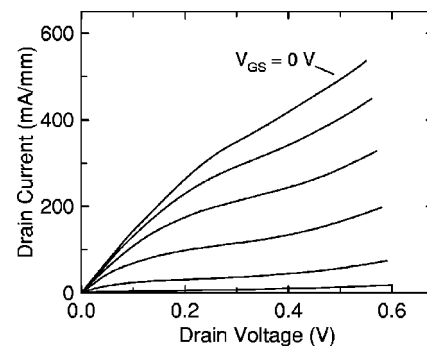
FIG. 3. Approximate band structure for InAs/AlSb/GaSb RITD based upon the bulk band offsets for the materials. Electrons with energy  $E$  tunnel from the InAs conduction band through the AlSb barrier, into the GaSb valence band, through the second barrier, and into the InAs conduction band.

achieved using a hydrofluoric acid/peroxide-based etch. This etch also formed a gate air bridge extending from the channel to the gate bonding pad.

### III. RESULTS AND DISCUSSION

A typical set of HEMT drain characteristics is shown in Fig. 4 for a device with a 0.1  $\mu\text{m}$  gate length, a 30  $\mu\text{m}$  gate width, and a 1  $\mu\text{m}$  source–drain spacing. The room-temperature carrier mobility and density are 23 000  $\text{cm}^2/\text{Vs}$  and  $1.2 \times 10^{12}/\text{cm}^2$ , respectively. The low-field source–drain resistance at  $V_{GS}=0$  V is 0.7  $\Omega$  mm, and the devices display good pinchoff at  $V_{GS}=-0.5$  V. We attribute the lack of saturation in the drain current primarily to the accumulation of holes generated by impact ionization in the channel that serves to reduce carrier depletion. A transconductance of 1.0 S/mm is measured at a source–drain voltage of only 300 mV. Using  $S$ -parameter measurements, a unity-current-gain cutoff frequency,  $f_T$ , of 160 GHz is obtained at  $V_{DS}=-0.5$  and  $V_{GS}=-0.35$  V. We subtracted the bonding pad capacitance and calculated an intrinsic  $f_T$  of 220 GHz.

A typical  $I$ – $V$  characteristic for the RITD in Fig. 1 is shown in Fig. 5. The device exhibits characteristic negative differential resistance, with a peak current of 180  $\mu\text{A}$  near 120 meV, valley currents of 16  $\mu\text{A}$  in the vicinity of 300 meV, and a peak-to-valley ratio of 11. The mesa size was 1.3  $\mu\text{m}$ , yielding peak current densities of  $1.4 \times 10^4$  A/cm<sup>2</sup>. The features in the negative resistance region are due to bistability effects.<sup>12</sup> Several similar RITDs (15 Å barriers and 80 Å wells) were grown directly on InAs substrates and GaAs sub-

FIG. 4. HEMT drain characteristics at room temperature for a device with  $L_g=0.1$   $\mu\text{m}$ ,  $L_{SD}=1$   $\mu\text{m}$ , and  $W_G=30$   $\mu\text{m}$ ;  $V_{GS}=0.1$  V/step. The device operates in the depletion mode, with pinch off near  $V_{GS}=-0.5$  V. RITD was grown above HEMT structure (see Fig. 1).

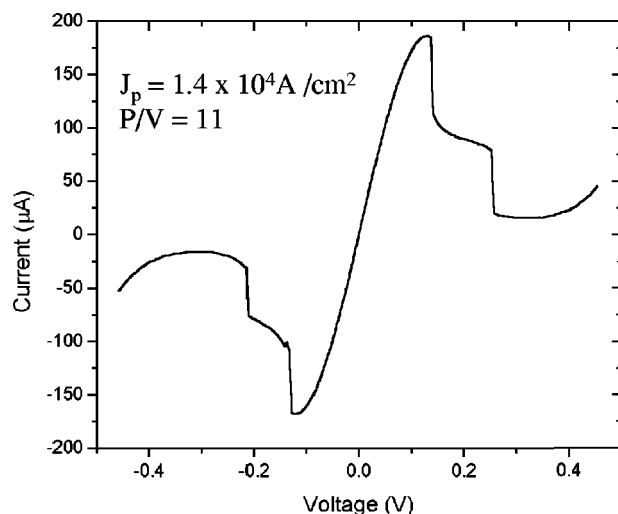


FIG. 5. Current as a function of bias voltage acquired at room temperature for 1.3  $\mu\text{m}$  diameter mesa RITD grown above HEMT structure (see Fig. 1).

strates with thick InAs buffer layers. Peak current densities ranged from  $1 \times 10^4$  A/cm<sup>2</sup> to  $3 \times 10^4$  A/cm<sup>2</sup> with peak-to-valley ratios of 10–15. Hence, it appears that growing an RITD above a HEMT results in little or no degradation of RITD performance. It is important to have high peak current densities because the speed of a RITD is roughly proportional to the peak current density divided by the junction capacitance. In our work on RITDs grown on GaAs and InAs substrates (without the HEMT), we have obtained higher peak currents and acceptable peak-to-valley ratios with thinner AlSb barriers (e.g., 9 Å). These results should apply to the RITD/HEMT structures as well.

We have found that the substrate temperature during MBE growth of the RITD/HEMT structure is critical for some layers but not for others. The AlSb buffer layer is typically grown near 550 °C. We have achieved high-mobility InAs/AlSb single quantum wells on AlSb buffer layers grown at temperatures from 500 to 600 °C; lower and higher temperatures may be suitable as well. The growth temperature for the InAs channel and subchannel, along with adjacent AlSb, is 500 °C. Substantially higher temperatures result in In desorption. InAs/AlSb single quantum wells grown at 400 °C exhibit lower electron mobility. The In-

As(Si) donor layer, however, must be grown near 400 °C to minimize Si segregation into the AlSb where it acts as an acceptor.<sup>8</sup> Poor surface morphology results if the etch stop and 1000–2000 Å InAs interlayers between the HEMT and RITD are grown at too high a temperature. Specifically, we have found that temperatures near 400–430 °C are suitable but higher temperatures are not. The RITDs were grown near 450 °C for the devices reported here. A separate study of RITDs on GaAs substrates with InAs buffer layers showed that device performance was relatively insensitive to growth temperature over a range of 350–500 °C.

The demonstration of working RITDs and HEMTs from a single heterostructure is an important step toward the fabrication of high-speed, low-power logic circuits in the 6.1 Å material system. The next step, which is in progress at our laboratory, is the design and fabrication of simple circuits to assess the performance potential of this approach.

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- <sup>1</sup>J. P. A. van der Wagt, A. C. Seabaugh, and E. A. Beam III, *IEEE Electron Device Lett.* **19**, 7 (1998).
- <sup>2</sup>K. Maezawa, H. Matsuzaki, M. Yamamoto, and T. Otsuji, *IEEE Electron Device Lett.* **19**, 80 (1998).
- <sup>3</sup>J. B. Boos, B. R. Bennett, W. Kruppa, D. Park, J. Mittereder, R. Bass, and M. E. Twigg, *J. Vac. Sci. Technol. B* **17**, 1022 (1999).
- <sup>4</sup>D. H. Chow, H. L. Dunlap, W. Williamson, S. Enquist, B. K. Gilbert, S. Subramaniam, P. M. Lei, and G. H. Bernstein, *IEEE Electron Device Lett.* **17**, 69 (1996).
- <sup>5</sup>W. Williamson, S. B. Enquist, D. H. Chow, H. L. Dunlap, S. Subramaniam, P. M. Lei, G. H. Bernstein, and B. K. Gilbert, *IEEE J. Solid-State Circuits* **32**, 222 (1997).
- <sup>6</sup>J. Shen, S. Tehrani, H. Goronkin, G. Kramer, and R. Tsui, *IEEE Electron Device Lett.* **17**, 94 (1996).
- <sup>7</sup>J. B. Boos, M. J. Yang, B. R. Bennett, D. Park, W. Kruppa, C. H. Yang, and R. Bass, *Electron. Lett.* **34**, 1525 (1998).
- <sup>8</sup>B. R. Bennett, M. J. Yang, B. V. Shanabrook, J. B. Boos, and D. Park, *Appl. Phys. Lett.* **72**, 1193 (1998).
- <sup>9</sup>J. B. Boos, W. Kruppa, B. R. Bennett, D. Park, S. W. Kirchoefer, R. Bass, and H. B. Dietrich, *IEEE Trans. Electron Devices* **45**, 1869 (1998).
- <sup>10</sup>B. V. Shanabrook, J. R. Waterman, J. L. Davis, and R. J. Wagner, *Appl. Phys. Lett.* **61**, 2338 (1992).
- <sup>11</sup>B. R. Bennett, B. V. Shanabrook, and E. R. Glaser, *Appl. Phys. Lett.* **65**, 598 (1994).
- <sup>12</sup>C. Y. Belhadj, K. P. Martin, S. B. Amor, J. J. L. Rascol, R. J. Higgins, R. C. Potter, H. Hier, and E. Hempfling, *Appl. Phys. Lett.* **57**, 58 (1990).